CLAIMS

Please amend the claims as follows:

1. (canceled)
2. (canceled)

3. (currently amended) The data transmission system according to Claim [[2]] 33, wherein each of said plurality of network adapters includes:

a clock multiplier for multiplying a data clock and for providing said control logic with timing pulses utilized to transmit said request signal (REQ).

4. (canceled)

5. (currently amended) The data transmission system according to Claim [[4]] 33, wherein said first data bytes designate a point-to-point connection, a multicast connection, or a broadcast connection.

6. (currently amended) The data transmission system according to Claim [[1]] 33, wherein said means for converting data frames into a bit stream of serial data comprises:

means for generating serial data in a high-level data link control (HDLC) format before transmitting said serial data to said crossbar switch.

7. (previously presented) The data transmission system according to Claim 6, wherein said means for generating serial data comprises:

means for generating a first flag to start a data frame;

means for serializing a plurality of incoming parallel data bytes;

means for computing a frame check sequence (FCS) after serializing said plurality of incoming parallel data bytes; and

means for generating a second flag to end the data frame.

8. (previously presented) The data transmission system according to Claim 6, wherein said means for converting a bit stream of serial data received from said crossbar switch into data frames comprises:

means for converting serial data received from the crossbar switch in the a high-level data link control (HDLC) format into local area network (LAN) data frames.

9. (previously presented) The data transmission system according to Claim 8, wherein said means for converting serial data received from said crossbar switch into data frames comprises:

means for checking data integrity by computing a frame check sequence (FCS).

10. (previously presented) The data transmission system according to Claim 9, wherein each of said plurality of network adapters further includes:

a memory including a network-to-switch area organized in a first plurality of buffers for storing data to be transmitted via said crossbar switch , and a switch-to-network area organized in a second plurality of buffers for storing data received from said crossbar switch.

11. (currently amended) The data transmission system according to Claim [[1]] 33, wherein each of said plurality of network adapters further includes:

an internal parallel bus coupled to the serial communication controller; and

a network controller , coupled to the internal parallel bus, for converting data received in serial format from an attached network into parallel data bytes and for transmitting the parallel data bytes to the serial communication controller via the internal parallel bus.

12. (previously presented) The data transmission system according to Claim 11, wherein said network controller further includes:

a clock circuit;

means for synchronizing said clock circuit during a set of preamble bytes when receiving an incoming data frame from an attached network;

means for detecting the incoming data frame through a delimiter byte;

means for checking data integrity of said incoming data frame by computing a set of frame check sequence (FCS) bytes;

means for removing protocol information of said incoming data frame; and

means for deserializing remaining incoming bits of said incoming data frame to provide a set of parallel data bytes.

13. (previously presented) The data transmission system according to Claim 11, wherein said network controller further includes:

means for serializing a set of incoming data bytes received from said serial communication controller;

means for generating protocol information bytes to be included in an outgoing data frame; and

means for computing a frame check sequence (FCS) of said outgoing data frame before transmitting said outgoing data frame on an attached network.

14. (previously presented) The data transmission system according to Claim 11, further comprising:

an arbiter for resolving contention between requests to send from said network controller and requests to send from said serial communication controller.

15. (currently amended) The data transmission system according to Claim [[1]] 33, wherein said crossbar switch further includes:

a scheduler for scheduling data transmission between attached networks based upon requests to transmit received from said plurality of adapters.

16. (previously presented) The data transmission system according to Claim 15, wherein said scheduler further includes:

an algorithm unit for determining the best data connection to establish based upon selection of a request amongst all requests concurrently received from said plurality of adapters which meets a predetermined criterion.

17. (canceled)

18. (canceled)

19. (currently amended) The data transmission system according to Claim [[18]] 34, wherein each of said plurality of LAN adapters includes:

a clock multiplier for multiplying a data clock and for providing said control logic with timing pulses utilized to transmit said request signal (REQ).

20. (canceled)

21. (currently amended) The data transmission system according to Claim [[20]] 34, wherein said first data bytes designate a point-to-point connection, a multicast connection, or a broadcast connection.

22. (currently amended) The data transmission system according to Claim [[17]] 34, wherein said means for converting parallel bytes of a LAN data frame comprises:

means for generating a high-level data link control (HDLC) frame before transmitting said HDLC frame to said ATM crossbar switch.

23. (previously presented) The data transmission system according to Claim 22, wherein said means for generating serial data comprises:

means for generating a high-level data link control (HDLC) flag to start said HDLC frame;

means for serializing a plurality of incoming parallel data bytes;

means for computing a frame check sequence (FCS) after said plurality of incoming parallel data bytes; and

means for generating another HDLC flag to end said HDLC frame.

24. (previously presented) The data transmission system according to Claim 22, wherein said serial communication controller further includes:

means for converting a high-level data link control (HDLC) frame received from said ATM crossbar switch into a LAN data frame.

25. (previously presented) The data transmission system according to Claim 24, wherein said means for converting a high-level data link control (HDLC) frame received from said ATM crossbar switch into a LAN data frame comprises:

means for detecting a starting high-level data link control (HDLC) frame in an incoming HDLC frame;

means for checking the data integrity of said HDLC frame by computing a frame check sequence (FCS); and

means for deserializing a plurality of data bits of said HDLC frame to provide a plurality of data bytes in said LAN data frame.

26. (previously presented) The data transmission system according to Claim 25, wherein each of said plurality of LAN adapters further includes:

a memory including a first LAN-to-switch area organized in a first plurality of buffers for storing LAN data frames to be transmitted to another LAN via the ATM crossbar switch, and a second switch-to-LAN area organized in a second plurality of buffers for storing LAN data frames received from another LAN via the ATM crossbar switch.

27. (currently amended) The data transmission system according to Claim [[17]] 34, wherein each of said plurality of LAN adapters includes:

an internal parallel bus coupled to the serial communication controller; and

a LAN controller, coupled to the internal parallel bus, for converting LAN data frames received in serial form from an attached LAN into parallel data bytes and for transmitting the parallel data bytes to the serial communication controller via the internal parallel bus.

28. (previously presented) The data transmission system according to Claim 27, wherein said LAN controller further includes:

a clock circuit;

means for synchronizing said clock circuit during a set of preamble bytes when receiving an incoming LAN data frame from an attached LAN;

means for detecting said incoming LAN data frame through a delimiter byte;

means for checking data integrity of said incoming LAN data frame by computing a set of frame check sequence (FCS) bytes;

means for removing protocol information of said incoming LAN data frame; and

means for deserializing remaining incoming bits of said incoming LAN data frames to provide a set of parallel data bytes.

29. (previously presented) The data transmission system according to Claim 27, wherein said LAN controller further includes:

means for serializing a set of incoming data bytes received from said serial communication controller;

means for generating protocol information bytes to be included in an outgoing LAN data frame; and

means for computing a frame check sequence (FCS) of said outgoing LAN data frame before transmitting said outgoing LAN data frame to an attached LAN.

30. (previously presented) The data transmission system according to Claim 27, further comprising:

an arbiter resolving contention between requests to send from said LAN controller and requests to send from said serial communication controller.

31. (currently amended) The data transmission system according to Claim [[17]] 34, wherein said ATM crossbar switch further includes:

a scheduler for scheduling data transmission between attached networks based upon requests to transmit received from said plurality of adapters.

32. (previously presented) The data transmission system according to Claim 31, wherein said scheduler further includes:

an algorithm unit for determining the best data connection to establish based upon selection of a request amongst all requests concurrently received from the plurality of LAN adapters which meets a predetermined criterion.

33. (previously presented) A data transmission system, comprising:

a crossbar switch;

a plurality of network adapters coupled for communication therebetween by said crossbar switch, wherein each of said plurality of network adapters includes:

a serial communication controller including:

means for converting data frames into a bit stream of serial data before transmitting said serial data to said crossbar switch; and

means for converting a bit stream of serial data received from said crossbar switch into data frames of parallel bytes before transmitting said data frames toward an attached network; and

control logic for generating a request signal (REQ) to said crossbar switch when said adapter requests transfer of data frames to another network adapter, wherein said request signal (REQ) includes first data bytes defining a destination address of data to be transmitted and second data bytes representing a connection time defined by a number of slots of said crossbar switch in which the data are to be transmitted, wherein:

said control logic comprises first control logic that generates said request signal (REQ) during a last time slot of a previous transmission via said crossbar switch;

said crossbar switch includes second control logic for generating a grant signal (GNT) to a network adapter during said last time slot of said previous transmission; and

said first control logic, responsive to receiving said grant signal (GNT), transmits data for said number of slots specified by said request signal (REQ) immediately after said last time slot of said previous transmission.

34. (previously presented) A data transmission system, comprising:

an asynchronous transfer mode (ATM) crossbar switch;

a plurality of local area network (LAN) adapters coupled for communication therebetween by said ATM crossbar switch, wherein each of said LAN adapters includes:

a serial communication controller including:

means for converting parallel data bytes of a LAN data frame into a bit stream of serial data implemented as concatenated slots of an ATM cell size in high-level data link control (HDLC) format before transmitting said serial data to said ATM crossbar switch; and

means for converting a bit stream of serial data implemented as concatenated ATM cells received from said ATM crossbar switch into parallel bytes of a LAN data frame before transmitting said LAN data frame toward an attached LAN; and

control logic for generating a request signal (REQ) to said ATM crossbar switch when said LAN adapter requests transfer of at least a LAN data frame to another LAN adapter, wherein said request signal (REQ) includes first data bytes defining a destination address of data to be transmitted and second data bytes representing a connection time defined by a number of slots of said ATM crossbar switch in which the data are to be transmitted, wherein:

said control logic comprises first control logic that generates said request signal (REQ) during a last time slot of a previous transmission via said ATM crossbar switch;

said crossbar switch includes second control logic for generating a grant signal (GNT) to a LAN adapter during said last time slot of said previous transmission; and

said first control logic, responsive to receiving said grant signal (GNT), transmits data for said number of slots specified by said request signal (REQ) immediately after said last time slot of said previous transmission.